WHAT IS CLAIMED IS:

1. A pattern forming method of forming a desired pattern on a semiconductor substrate comprising:

extracting a first pattern of a layer;

extracting a second pattern of one or more layers overlapped with the layer, the second pattern being arranged close to or overlapped with the first pattern;

calculating a distance between the first and second patterns on a semiconductor substrate in consideration of a predetermined process variation;

determining whether or not the distance between the first and second patterns satisfy an allowable margin given for the distance between the first and second patterns; and

correcting, if the distance does not satisfy the allowable margin, at least one of the first and second patterns to satisfy the allowable margin.

2. The pattern forming method according to claim 1, wherein the first and second patterns comprise one of a design pattern and a mask pattern formed on a mask, and the layers includes the patterns concurrently arranged each other.

3. The pattern forming method according to claim 1, wherein the process variation includes at least one of a variation of an exposure quantity of an exposure apparatus, a variation of a focal distance, a variation of an exposure irradiation, a variation of

a lens aberration, a variation of a mask dimension, a variation of a development process, and a variation of an etching process.

4. The pattern forming method according to claim 1, wherein the first and second patterns satisfies a predetermined design rule.

5. The pattern forming method according to claim 1, wherein, if the first and second patterns are first and second design patterns, correcting at least one of the first and second patterns to satisfy the allowable margin is correcting the first and second design patterns to satisfy a predetermined design rule.

6. The pattern forming method according to claim 1, wherein correcting at least one of the first and second patterns to satisfy the allowable margin is widening dimensions of the first and second patterns.

7. The pattern forming method according to claim 1, wherein a minimum distance between the first and second patterns after correcting at least one of the first and second patterns satisfies a predetermined minimum width.

8. The pattern forming method according to claim 4, wherein the predetermined design rule is defined by lithography simulation or experiment.

9. The pattern forming method according to claim 1, wherein, after correcting at least one of the first and second patterns, features including

extracting, determining and correcting recited in claim 1 are carrying out for another first pattern and another second pattern.

10. A mask pattern forming method of forming a desired pattern on a semiconductor substrate comprising:

extracting a first design pattern of a layer;

extracting a second design pattern of one or more layers overlapped with the layer, the second design pattern being arranged close to or overlapped with the first design pattern;

correcting the first design pattern in accordance with a correction rule of a design pattern defined by at least one of widths of the first and second design patterns on one hand and a distance between the first and second design patterns on the other hand; and

forming a mask pattern by further correcting the first design pattern having corrected in accordance with the correction rule, by process proximity effect correction.

11. The mask pattern forming method according to claim 10, wherein, following extracting the first design pattern,

extracting a third pattern which is present in the layer in which the first pattern is present, the third pattern being arranged close to the first pattern; and

correcting the first design pattern in accordance

with a correction rule of a design pattern defined by at least one of widths of the first and third design patterns on one hand and a distance between the first and third design patterns on the other hand.

12. The mask pattern forming method according to claim 10, wherein the process proximity effect correction includes at least one of correction for a variation of an etching process, correction for a variation of a lithography process, and correction for a variation of a mask process.

13. A pattern forming system of forming a desired pattern on a semiconductor substrate comprising:

an extracting section configured to extract a first pattern of a layer;

an extracting section configured to extract a second pattern of one or more layers overlapped with the layer, the second pattern being arranged close to or overlapped with the first pattern;

a calculating section configured to calculate a distance between the first and second patterns on a semiconductor substrate in consideration of a predetermined process variation;

a determining section configured to determine whether or not the distance between the first and second patterns satisfy an allowable margin given for the distance between the first and second patterns; and

a correcting section configured to correct, if the

distance does not satisfy the allowable margin, at least one of the first and second patterns to satisfy the allowable margin.

14. The pattern forming system according to claim 13, wherein the first and second patterns comprise one of a design pattern and a mask pattern formed on a mask, and the layers includes the patterns concurrently arranged each other.

15. The pattern forming system according to claim 13, wherein the process variation includes at least one of a variation of an exposure quantity of an exposure apparatus, a variation of a focal distance, a variation of an exposure irradiation, a variation of a lens aberration, a variation of a mask dimension, a variation of a development process, and a variation of an etching process.

16. The pattern forming system according to claim 13, wherein the first and second patterns satisfies a predetermined design rule.

17. The pattern forming system according to claim 13, wherein, if the first and second patterns are first and second design patterns, correcting at least one of the first and second patterns to satisfy the allowable margin is correcting the first and second design patterns to satisfy a predetermined design rule.

18. The pattern forming system according to claim 13, wherein correcting at least one of the first

and second patterns to satisfy the allowable margin is widening dimensions of the first and second patterns.

19. The pattern forming system according to claim 13, wherein a minimum distance between the first and second patterns after correcting at least one of the first and second patterns satisfies a predetermined minimum width.

20. The pattern forming system according to claim 16, wherein the predetermined design rule is defined by lithography simulation or experiment.

21. The pattern forming system according to claim 13, wherein, after correcting at least one of the first and second patterns, features including extracting, determining and correcting recited in claim 1 are carrying out for another first pattern and another second pattern.

22. A mask pattern forming system of forming a desired pattern on a semiconductor substrate comprising:

an extracting section configured to extract a first design pattern of a layer;

an extracting section configured to extract a second design pattern of one or more layers overlapped with the layer, the second design pattern being arranged close to or overlapped with the first design pattern;

a correcting section configured to correct the

first design pattern in accordance with a correction rule of a design pattern defined by at least one of widths of the first and second design patterns on one hand and a distance between the first and second design patterns on the other hand; and

a forming section configured to form a mask pattern by further correcting the first design pattern having corrected in accordance with the correction rule, by process proximity effect correction.

23. The mask pattern forming system according to claim 22, further comprising

an extracting section configured, following extracting the first design pattern, to extract a third pattern which is present in the layer in which the first pattern is formed, the third pattern being arranged close to the first pattern; and

a correcting section configured to correct the first design pattern in accordance with a correction rule of a design pattern defined by at least one of widths of the first and third design patterns on one hand and a distance between the first and third design patterns on the other hand.

24. The mask pattern forming system according to claim 22, wherein the process proximity effect correction includes at least one of correction for a variation of an etching process, correction for a variation of a lithography process, and correction

for a variation of a mask process.

25. A method of manufacturing a semiconductor device comprising:

extracting a first pattern of a layer;

extracting a second pattern of one or more layers overlapped with the layer, the second pattern being arranged close to or overlapped with the first pattern;

calculating a distance between the first and second patterns on a semiconductor substrate in consideration of a predetermined process variation;

determining whether or not the distance between the first and second patterns satisfy an allowable margin given for the distance between the first and second patterns;

correcting, if the distance does not satisfy the allowable margin, at least one of the first and second patterns to satisfy the allowable margin;

forming an exposure mask according to the at least one corrected pattern; and

forming a semiconductor device on the semiconductor substrate via a lithography process by using the exposure mask.

ABSTRACT OF THE DISCLOSURE

A pattern forming method of forming a desired pattern on a semiconductor substrate is disclosed, which comprises extracting a first pattern of a layer, extracting a second pattern of one or more layers overlapped with the layer, the second pattern being arranged close to or overlapped with the first pattern, calculating a distance between the first and second patterns on a semiconductor substrate in consideration of a predetermined process variation, determining whether or not the distance between the first and second patterns satisfy an allowable margin given for the distance between the first and second patterns, and correcting, if the distance does not satisfy the allowable margin, at least one of the first and second patterns to satisfy the allowable margin.